Remarks

Claims 1-20, and 22-35 remain in the application. Claims 1, 19 and 35 have been amended.

Claim Rejections—35 USC 102

Examiner rejected claims 1-35 under 35 USC 102(e) as being anticipated by Arnold et al. (US Pat. No. 6,438,681) herein referred to as Arnold.

Regarding claim 1, Applicant's claim 1, as amended, recites the following:

"A method of monitoring and controlling instruction dependency for microprocessors, the method comprising: fetching an instruction at a thread control element from an instruction buffer; comparing, with a comparator, one or more source operand identifications of the instruction at the thread control element outside of a pipeline stage or storage location to one or more temporary register identifications, wherein each thread control element and comparator forms a bi-directional correspondence, and wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations; verifying whether any of the one or more source operand identifications at the thread control element matches any of the one or more temporary register identifications; and in response to a match of the source operand identification and the temporary register identification, prohibiting the instruction held in the corresponding thread control element from executing in that clock cycle, wherein the match corresponds to instruction dependency."

Regarding claim 1, examiner has rejected claim 1 as being anticipated by Arnold. In order to anticipate an invention under 35 USC 102(e), the cited reference must contain all the limitations of a particular claim that the reference is deemed to anticipate. Claim 1 of Applicant's teaching discloses "comparing, with a comparator, one or more source operand identifications of the instruction at the thread control element outside of a pipeline stage or storage location to one or more temporary register identifications, wherein each thread control element and comparator forms a bi-directional correspondence, and wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations;". Applicant's claim 1 teaches comparing source operand identifications at the thread control element *outside of a pipeline stage or storage location* to temporary register identifications *in* the pipeline storage location. Applicant's claim 1 further teaches each thread control element and comparator as having a bi-directional correspondence. The cited reference of Arnold does not teach of a comparator having any correspondence with a thread control element, let alone a bi-directional correspondence. Neither does the cited reference teach of a thread control element outside of a pipeline stage or storage location. Additionally, the cited reference (col. 6, lines 58-62) teaches "the comparison logic **24** compares the n-bit register identifier of the consumer in the register stage **25** with each of the n-bit register identifiers of producers in the execution stage **28**, the detect exceptions stage **32**, and the write stage **35**." Clearly, the cited reference of Arnold discloses comparison logic that specifically compares data in one stage of a pipeline to other stages of the same pipeline. Determining whether a data dependency or data dependency hazard exists takes place in

the pipeline itself. An earlier stage of the pipeline or pipelines is compared with later stage/stages of the pipeline or pipelines to check if data dependency hazards exist or not.

Claim 1 of Applicant's teaching recites a verification step to check if source operands at the thread control elements match any of the one or more temporary register identifications stored in one or more temporary register identification pipeline storage locations, respectively. In contrast, the cited reference discloses a comparator which takes one stage of the pipeline and compares it with other stages of the same pipeline to determine a data dependency hazard. In applicant's teaching, the comparator is comparing the source operand in the thread control element with a temporary register identification stored in a temporary register identification pipeline storage location. Claim 1 further recites a fetching operation at the thread control element from an instruction buffer. If an analogy were to be drawn from examiner's citation of "instruction dispersal unit" it could be compared with Applicant's instruction buffer. The thread control unit, having bi-directional correspondence with a comparator is indeed an innovation over prior art.

Thus, Applicant's claim 1 is not anticipated by the cited reference. Consequently, and in light of the above, applicant respectfully requests that a 102(e) rejection to claim 1 be withdrawn and a notice of allowance be made.

Regarding claims 2-18, claims 2-18 are dependent upon claim 1, and as shown above, Applicant's claim 1 is not anticipated by the cited reference of Arnold. Therefore claims 2-18 are not anticipated by Arnold for at least the same reasons as claim 1. Consequently, and in light of the above, Applicant requests that a 102(e) rejection to claims 2-18 be withdrawn and a notice of allowance be made.

Regarding claim 19, examiner has rejected claim 19 as being anticipated by Arnold. In order to anticipate an invention under 35 USC 102(e), the cited reference must contain all the limitations of a particular claim that the reference is deemed to anticipate. Claim 19 of Applicant's teaching recites "fetching an instruction at a thread control element". Examiner has mistaken the thread control element for an instruction dispersal unit. This is factually incorrect because Applicant's claim 19 teaches fetching of an instruction from an instruction buffer. Therefore, there is no fetching unit outside the pipeline in the cited reference, and the instruction buffer in Applicant's claim 19 could be construed as an instruction dispersal unit of the cited reference. It is the disclosed pipeline of the cited reference which fetches instructions from the instruction dispersal unit. On the other hand the thread control applicant's teaching, not part of the pipeline, fetches instructions from an instruction buffer.

Applicant's claim 19 recites a comparison step wherein "source operand identifications of the instruction at the thread control element" are compared to "one or more temporary register identifications, wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline[[s]] storage locations;" The cited reference (col. 6, lines 58-61) only discloses "the comparison logic **24** compares the n-bit register identifier of the consumer in the register stage **25** with each of the n-bit register identifiers of producers in the execution stage **28**, the detect exceptions stage **32**, and the write stage **35**." Essentially the comparator of the cited reference is used to compare one stage of the pipeline to all other stages of the same pipeline. This is in contrast to Applicant's claim 19 wherein comparison step is between

"one or more source operand identifications" of an instruction at a thread control unit not part of the pipeline, and "one or more temporary register identifications" stored in a "temporary register identification pipeline storage location". Again, claim 19 recites a verification step to check if source operands at the thread control elements match any of the one or more temporary register identifications stored in one or more temporary register identification pipeline storage locations, respectively. In contrast, the cited reference (col. 6, line 66—col 7, line 10) discloses a comparator which takes one stage of the pipeline and compares it with other stages of the same pipeline to determine if there is a match, and thus a data dependency hazard. Applicant's claim 19 is not anticipated because Applicant teaches comparing the source operand in the thread control element, not part of the pipeline, with a temporary register identification stored in a temporary register identification pipeline storage location, which is part of the pipeline.

Applicant's claim 19 further recites "writing a null value into a first pipeline storage location" if "the destination operand of the instruction is not a temporary register". Examiner has cited col 6, lines 35-49, and Fig. 2, component 87 of Arnold as grounds for rejection of the above. The reference cited does not state that a null value is written into a first pipeline storage location if the destination operand is not a temporary register. The reference merely states that the "n-bit register identifier is latched into stages **25**, **28**, **32**, and **35** by latches **87**, **89**, **91** and **93**, respectively, on the same edges that the instruction is respectively latched into stages **25**, **28**, **32**, and **35**." Further, Fig. 2, which examiner has cited as anticipating Applicant's claim 19, does not have any component 87. Applicant thus respectfully states that examiner is in error.

Applicant's claim 19 is therefore, not anticipated by the cited reference. Consequently, in light of the above, Applicant respectfully requests that a 102(e) rejection to claim 19 be withdrawn and a notice of allowance be made.

Regarding claims 20-28, claim 20 and claims 22-28 are dependent upon claim 19, and as shown above, Applicant's claim 19 has not been anticipated by the cited reference of Arnold. Therefore, claims 20 and claims 22-28 are not anticipated by Arnold for at least the same reasons as claim 19. Consequently, Applicant respectfully requests that a 102(e) rejection to claim 20 and claims 22-28 be withdrawn and a notice of allowance be made.

Claim 21 has been cancelled.

Regarding claim 29, examiner has rejected claim 29 as being anticipated by Arnold. Claim 29 of Applicant's teaching recites "A system for instruction dependency monitor and control, comprising: a set of one or more thread control elements for fetching instructions, wherein said thread control elements are not part of a pipeline stage or pipeline storage location; a set of one or more comparing elements, wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements; and a set of one or more temporary register identification pipeline storage locations, wherein the one or more temporary register identification pipeline storage locations are directly coupled to the one or more comparing elements."

In order to anticipate an invention under 35 USC 102(e), the cited reference must contain all the limitations of a particular claim that the reference is deemed to anticipate. Claim 29 recites a set of one or more thread control elements for fetching instructions.

This is not recited by the cited reference (col. 3, lines 13-23). The cited reference only discloses an instruction dispersal unit, not a thread control element. If at all an analogy is drawn with the cited reference, it would be similar to Applicant's instruction buffer, taught in the specification (page 12, lines 16-17) not recited in claim 29. Further, comparing elements, recited in claim 29 are coupled directly to thread control elements, unlike the cited reference where comparison logic compares register identifier in "the register stage **25** with each of the n-bit register identifiers…in the execution stage **28**, the detect exceptions stage **32**, and the write stage **35**." Essentially, comparison logic is used for comparison between the n bit register identifier of one stage of the pipeline with the register identifiers of the other stages of the same pipeline to compare various stages within a pipeline, and is not coupled to either an instruction dispersal unit or to a "thread control element" for fetching instructions. Applicant respectfully states that examiner is in error. Examiner would kindly appreciate that the thread control elements are not part of the pipeline, but the instruction held in the thread control element is compared with the temporary register identifier of the pipeline storage location in the pipeline for data dependency.

Consequently, and in light of the above, Applicant's claim 29 is not anticipated by the cited reference of Arnold. Therefore, Applicant respectfully requests a 102(e) rejection to claim 29 be withdrawn and a notice of allowance be made.

Regarding claims 30-34, claims 30-34 are dependent upon claim 29 and as shown above, claim 29 is not anticipated by the cited reference of Arnold for at least the same reasons as claim 29. Therefore, claims 30-34 are not anticipated by Arnold.

Consequently, Applicant respectfully requests that a 102(e) rejection to claims 30-34 be withdrawn and a notice of allowance be made.

Regarding claim 35, examiner has rejected claim 35 as being anticipated by Arnold. Claim 35 of Applicant's teaching recites "A system for instruction dependency monitor and control, comprising: a set of one or more thread control elements for fetching instructions wherein said thread control elements are not part of a pipeline stage or storage location; a set of one or more comparing elements, wherein each of the one or more comparing elements is directly coupled to a corresponding thread control element in the set of one or more thread control elements and wherein each thread control element and comparing element forms a bi-directional correspondence; a set of one or more temporary register identification pipeline storage locations, wherein the one or more temporary register pipeline storage locations are directly coupled to the one or more comparing elements, and an arbiter coupled to the thread control elements, the comparing elements, and the temporary register pipeline storage locations in each stage of a pipeline or pipelines."

In order to anticipate an invention under 35 USC 102(e), the cited reference must contain all the limitations of a particular claim that the reference is deemed to anticipate. Claim 35 recites a set of one or more thread control elements for fetching instructions. This is not recited by the cited reference (col. 3, lines 13-23). The cited reference only discloses an instruction dispersal unit, not a thread control element. If at all an analogy is drawn with the cited reference, it would be similar to Applicant's instruction buffer, taught in the specification (page 12, lines 16-17) not recited in claim 35. Further, comparing elements, recited in claim 35 are coupled directly to thread control elements,

unlike the cited reference where comparison logic compares register identifier in "the register stage **25** with each of the n-bit register identifiers…in the execution stage **28**, the detect exceptions stage **32**, and the write stage **35**." Essentially, comparison logic is used for comparison between the n bit register identifier of one stage of the pipeline with the register identifiers of the other stages of the same pipeline to compare various stages within a pipeline, and is not coupled to either an instruction dispersal unit or to a "thread control element" for fetching instructions. Applicant respectfully states that examiner is in error. Examiner would kindly appreciate that the thread control elements are not part of the pipeline, as recited by amended claim 35, but the instruction held in the thread control element is compared with the temporary register identifier of the pipeline storage location in the pipeline for data dependency.

Further, Applicant would like to reassert that the cited reference does not disclose an arbiter coupled to thread control elements, comparing elements, and the temporary register pipelines. Support is found for Applicant's claim 35 wherein in the specification it is recited that "the arbiter **107** receives a match alert from a comparator, the arbiter prohibits the instruction held in the corresponding thread control element from executing in that clock cycle." (Page 9, lines 4-6). Examiner tries to draw an analogy between the instruction dispersal unit of the cited reference and the arbiter of Applicant's claim 35. Such an analogy is incorrect. Applicant's claim 35 teaches of an arbiter coupled to the thread control elements, comparing elements, and the temporary register pipelines. Neither figure 1 nor figure 3 of the cited reference show the instruction dispersal unit coupled to the comparison logic. Further, the cited text does not teach of the instruction dispersal unit either monitoring or controlling instruction dependency.

Consequently, and in light of the above, Applicant's claim 35 is not anticipated by the cited reference. Therefore, Applicant respectfully requests that a 102(e) rejection to claim 35 be withdrawn and a notice of allowance be made.

Response to Arguments

Examiner alleged that applicant's arguments for claims 1-18 and 29-34 amounts to general allegations that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant has rewritten the arguments to specifically point out Applicant's claims' distinguishing features over cited prior art. Further claims 1 and 29 have been amended to make explicit the fact that the thread control element is not part of the pipeline. Applicant believes that claims 1-18, and 29-34 are now in order of acceptance.

Regarding claims 19-28, claim 19 has been amended to explicitly state that "one or more source operand instructions at said thread control element is not part of a pipeline or pipelines". Applicant believes that amended claim 19 is in order of acceptance, and by thus virtue dependent claims 20, and 22-28 are also in order of acceptance.

Regarding claim 35, claim 35 has been amended to explicitly state that the comparing elements are directly coupled to their corresponding thread control elements. Claim 35 has also been amended to make explicit the fact that the thread control element is not part of the pipeline. Applicant believes that amended claim 35 is now in order of acceptance.

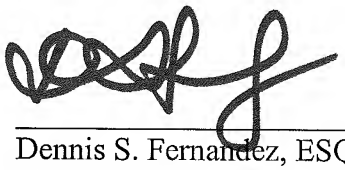
CONCLUSION

In view of the foregoing, the Applicant believes that all of the claims are now in condition for allowance and respectfully request the Examiner to issue a timely Notice of Allowance in this case. If for any reason, the Examiner believes any of the claims are not in condition for allowance, he is encouraged to call the undersigned attorney at 650-325-4999 so that any remaining issues may be resolved.

The above changes are believed not to add new matter, as support is found in the specification as described above.

Claims 1-20, and 22-35 remain in this application. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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